Claim 20, line 1, delete "17" and insert -- 11 --.

Please cancel claims 13, 15, 17, 35-43 without prejudice or disclaimer of the matter therein.

Claim

Please add new claims 44-48 as follows:

-- 44. A graphic processing apparatus comprising:

a memory for storing graphic data;

a data processor for executing a predetermined graphic processing to generate graphic data;

output means for outputting the graphic data stored in said memory;

a memory controller for controlling data transfer between said memory and said data processor in accordance with a request from said data processor;

a first bus, having m (wherein m is an integer) bits width, connected between said memory and said memory controller, for transferring m bits data in parallel; and

a second bus, having n (n is an integer, n > m) bits width, connected between said memory controller and said data processor, for transferring n bits data in parallel;

wherein said memory controller comprises:

a storage for temporarily storing graphic data read out from said memory in a time shared fashion through said first bus,

means for supplying said temporarily stored graphic data to said data processor as n bits parallel data, and

a converter for converting said temporarily stored graphic data into serial data which is provided to said output means.

45. An apparatus according to claim 44, wherein said memory controller further comprises:

a multiplexer for outputting the n bits graphic data transferred from said data processor to said first bus having m bits width in a time shared fashion.

46. An apparatus according to claim 44, wherein said memory controller further comprises:

means for generating an address signal for accessing said memory plural times, in response to a signal for accessing said memory supplied from said data processor.

47. An apparatus according to claim 44, wherein graphic data to be transferred to said memory controller through said first bus is read out from said memory plural times within a unit transfer time in a time shared fashion, based on an access signal to said memory designated by said data processor.

48. An apparatus according to claim 47, wherein the graphic data transferred to said memory controller is supplied to said data processor through said second bus within a time longer than twice said unit transfer time.